CURRICULUM VITAE

Ponzina Flavio

Personal Information

San Diego, California 92122
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Born: 31/01/1994
Languages: Italian (native), English (fluent), French (B2)
Hobby/interests: track and field, modern physics, history, and philosophy

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Publications: Flavio Ponzina - Google Scholar

Education

08/2019 – 09/2023
PhD student at Embedded Systems Laboratory (ESL)
Thesis – *Hardware-Software co-design Methodologies Edge AI Optimization.*

09/2016 – 12/2018
Master's Degree in Computer Engineering - *Embedded systems*
Thesis: *Hardware-Aware Optimization of Embedded CNNs.* - 110/110 *cum laude*

09/2013 – 07/2016
Bachelor's degree in Computer Engineering - 99/110

09/2008 – 07/2013
High school – Istituto tecnico industriale ITIS PININFARINA
Computer Science, Electronics - 100/100 *cum laude*

Work Experience

10/2023 – 09/2025
Post-doctoral researcher at University of California, San Diego (UCSD)
Large scale and in- and near-memory/storage processing systems

02/2019 – 07/2019
Internship with Embedded Systems Laboratory at EPFL.
Exploration and development of flexible, reusable and optimized hardware architectures to implement bio-signal processing and machine learning algorithms with ultra-low energy consumption

02/2017 – 04/2018
Software Engineer at PJM S.r.l.
Software development, network management, trainer of PHP/MySQL internal courses

09/2012 – 01/2017
ICT Consultant at MC TEAM.
Software development, feasibility studies, network management

06/2012 – 07/2012
Traineeship at MC TEAM.
Software development

List of Publications

- B. W. Denkinger *et al.*, *"Impact of Memory Voltage Scaling on Accuracy and Resilience of Deep Learning Based Edge Devices*," *IEEE Design & Test*, vol. 37, no. 2, pp. 84-92, 2020.
- M. Rios *et al.*, "*Running Efficiently CNNs on the Edge Thanks to Hybrid SRAM-RRAM In-Memory Computing*," *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, pp. 1881-1886, 2021.
- F. Ponzina *et al*, "*E2CNNs: Ensembles of Convolutional Neural Networks to Improve Robustness Against Memory Errors in Edge-Computing Devices*," *IEEE Transactions on Computers*, vol. 70, no. 8, pp. 1199-1212, 2021
- F. Ponzina *et al.*, "*A Flexible In-Memory Computing Architecture for Heterogeneously Quantized CNNs*," 2021 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Tampa, FL, USA, 2021, pp. 164-169, 2021.
- F. Ponzina *et al.*, "*Using Algorithmic Transformations and Sensitivity Analysis to Unleash Approximations in CNNs at the Edge*," Micromachines (Basel), 2022.
- M. Rios *et al.*, "*Error Resilient In-Memory Computing Architecture for CNN Inference on the Edge*," Proceedings of the Great Lakes Symposium on VLSI 2022 (GLSVLSI '22). Association for Computing Machinery, New York, NY, USA, 249–254, 2022.
- F. Ponzina *et al.*, "*An Accuracy-Driven Compression Methodology to Derive Efficient Codebook-Based CNNs*," *2022 IEEE International Conference on Omni-layer Intelligent Systems (COINS)*, Barcelona, Spain, pp. 1-6, 2022.
- F. Ponzina *et al.*, "*A Hardware/Software Co-Design Vision for Deep Learning at the Edge*," IEEE Micro, vol. 42, no. 6, pp. 48-54, Nov.-Dec. 2022.
- M. Rios *et al.*, "*Bit-Line Computing for CNN Accelerators Co-Design in Edge AI Inference,"* IEEE Transactions on Emerging Topics in Computing, 2023.
- S. Zanoli et al., "*An error-based approximation sensing circuit for event-triggered, low power wearable sensors*," IEEE JETCAS 2023
- F. Ponzina et al., "*Overflow-free compute memories for edge ai acceleration*," ACM Transactions on Embedded Computing Systems (TECS), ACM New York, NY, USA, 2023.

Master's degree course projects

- Testing and fault tolerance - *"Development of a suite of software self-test procedures for the RI5CY pipelined processor"* – 2018
- Bioinformatics - *"Exploring SIMD vectorization for TGS algorithms"* – 2018
- System design project - *"IP-Core Manager for FPGA-based design"* – 2018
- Microelectronic Systems - *"Design and Development of DLX Microprocessors in VHDL"* – 2017
- Specification and simulation of digital systems - *"Design and simulation of a system on chip"* - 2017

Research domain/interests

- Hardware-software co-design optimizations
- Artificial intelligence, machine learning, deep learning
- AI for biomedical applications
- Edge AI
- Federated learning
- Hardware accelerators
- In-memory computing
- ML for space applications and Earth observation