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Switched capacitor based Z-source DC–DC converter

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Abstract: This study proposes a common grounded Z-source DC–DC converter. In comparison to conventional Z-source converter, it converts voltage with higher voltage gain and lower voltage stress on the switch, diodes and capacitors. In addition, it needs smaller inductors in comparison to the similar converters. The converter is analysed and compared with other converters. Its main equations are obtained which show the converter advantages as lower voltage stresses, smaller inductors, higher efficiency and higher voltage gain in comparison to the reviewed converters. A prototype for the proposed converter is prepared based on analysis and theoretical parts. Experiments are done along the lines of the analysis. Experimental results and theoretical equations are used to prove the converter operation quality.

1 Introduction

Most of the renewable energy sources need DC–DC converters to boost the low voltage from the renewable energy side to high voltage on the load side [1–5]. Traditional boost converter is the first choice of non-isolated DC–DC converters which increases voltage with infinite limitation based on its voltage gain equation. However, its boosting mode has limitations that occur due to the parasitic resistances and voltage drop on the components [2–5]. Even if, the classical boost converter has a simple and cost effective structure, it cannot be used for high power applications and voltage stress on its components is high [6].

To solve these problems, new structures have been proposed that can be selected for different applications according to their positive and negative points [7–9]. The simplest method is cascading a boost converter that has some disadvantages as: low efficiency, high cost, high voltage drop, requiring many components and complex circuit [7]. The advantages of cascading boost converters are high voltage gain and reduction of voltage stress on the components. The other method is using a coupled inductor instead of the boost inductor [8, 9]. The turn ratio of the coupled inductor defines voltage gain. Thus, the converter requires a high turn ratio to operate with high voltage gain that imposes extra conduction loss, a leakage inductance and a big size inductor for the converter [5]. To overcome these problems, additional components like inductors, capacitors and diodes should be used as proposed in [5]. The other kind of extended converter based on boost is quadratic boost converter which consists of a reformed cascaded boost converter [10–12]. Its voltage gain is low and can be improved by adding a coupled inductor. However, the turn ratio of the inductor matches its voltage gain with the desired value, the converter suffers from increased voltage stress on its components due to the inductor's leakage inductance [10].

Other than the introduced methods and multiplier techniques, some new methods and structures have been proposed to improve operation and voltage gain [13–18]. The methods include utilising switched inductor and switched capacitor techniques to increase voltage gain of different converters [12, 16]. In addition, using interleaved converter configurations causes high voltage gain and reduction of voltage stress [17]. Although the methods have advantages, they are costly and bulky that encourage researchers to present new converters with novel configurations.

A cost effective and efficient converter was proposed in [19], which was called Z-source DC–DC converter. By using two inductors and two capacitors, a Z-source network can be implemented. The inductors and capacitors of the Z-source have connections in X-shape that makes possibilities to combine the Z-source network with the other converters and techniques like boost converter, switched inductor and switched capacitor [20]. The basic Z-source converter has no common ground; therefore its applications are limited. In [21], a switched inductor has been combined with the Z-source network thereby improving the voltage gain. However, the combination has drawbacks and it is a costly, complex and bulky solution. The other option is applying a switched capacitor to a Z-source DC–DC converter [22]. Similar to the previous case, the combination makes a complex and costly converter that has no common ground. By combining the switched capacitor technique with quasi-Z-source and Z-source, the structures do not need additional active switch. In addition, voltage gain and power can be increased [22]. The other proposed structures have focused on making the converter common grounded and reducing the voltage stress [23, 24]. A quasi-Z source converter is the new kind of converter retrieved from Z-source converter [2]. Using the quasi-Z source structure voltage stress is reduced and the converter has a common ground [2, 25]. Similar to the Z-source, quasi-Z source can be combined with the other techniques as switched capacitor to improve the converter characteristics as voltage gain and voltage stress [2].

This paper presents a new DC–DC converter topology utilising the Z-source network and switched capacitor that is common grounded and its voltage gain is higher than similar converters. The proposed converter has important advantages as reduced voltage stress on components, higher efficiency and using smaller minimum inductance for the inductors in comparison to the converters that include a Z-source network. To prove the positive points of the proposed converter, first it has been analysed. The obtained equations are used to compare the converter with the other converters and show its advantages. Then, a prototype is built to validate the converter operation by experimental result.

2 Analysis of the proposed converter

The proposed converter consists of the reformed conventional Z-source converter and additional components (two diodes and one capacitor). To achieve improvements in the boosting operation of the conventional Z-source converter, this paper presents a new structure which is analysed and compared with similar converters. As it is obvious in Fig. 1*a*, the proposed converter has a common

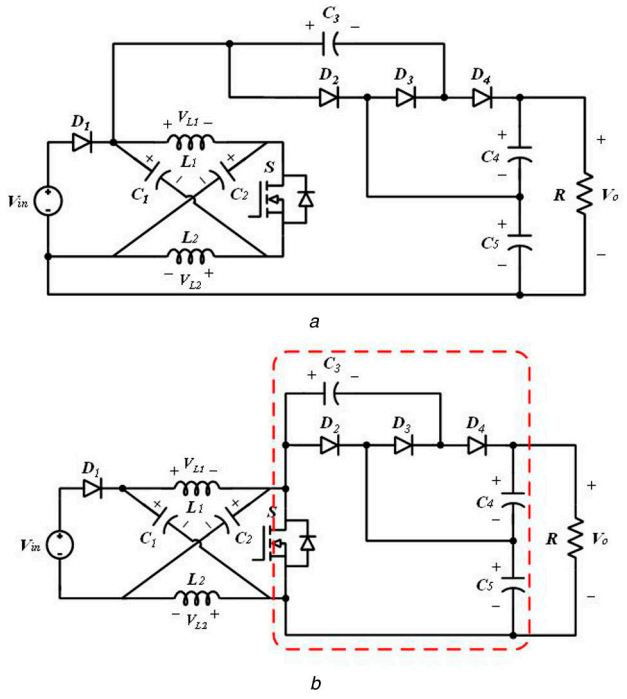

Fig. 1 *Configurations based on Z-source converter*
(a) Configuration of the proposed converter, ***(b)*** Combination of conventional Z-source and switched capacitor

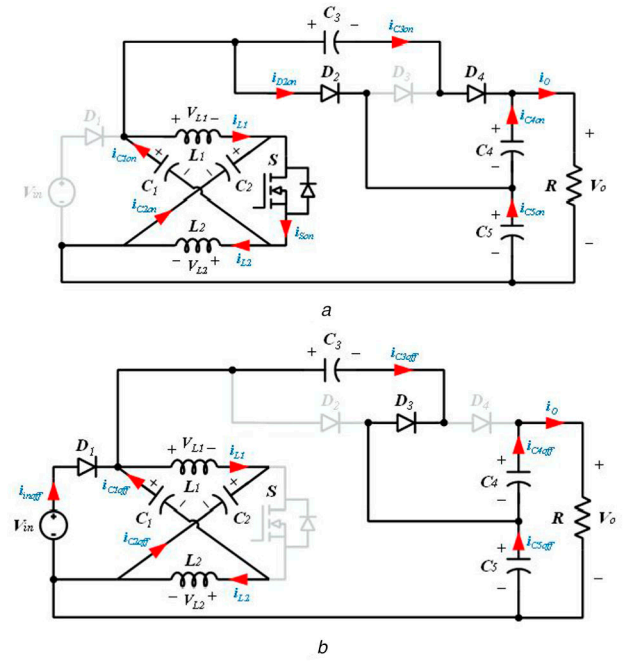

Fig. 2 *Switch on and off states for the proposed converter*
(a) First stage, switch is on, ***(b)*** Second stage, switch is off

ground and its parallel capacitor with the load is divided into two capacitors which are common with the switched capacitor. The common capacitors decrease the number of the converter components.

The other positive point of the proposed converter is method of using switched capacitor to increase voltage gain effectively. The other combination has been investigated which is not effective as the proposed one. The second possible combination of Z-source and switched capacitor is not common grounded as shown in Fig. 1*b*. Furthermore, the second combination voltage gain is lower than the proposed one. Equations (1) and (2) show voltage gain of the converters in Figs. 1*a* and *b*, respectively

$$M = \frac{V_o}{V_{in}} = \frac{3 - 2D}{(1 - 2D)} \tag{1}$$

$$M = \frac{V_o}{V_{in}} = \frac{2}{(1 - 2D)} \tag{2}$$

where D is duty cycle of the power switch.

The converters based on Z-source network operate in $0 \le D \le 0.5$. According to (1) and (2), it can be written $3 - 2D \ge 2$. Thus, the proposed converter has higher voltage gain.

It has to be noticed, the power switch's duty cycle defines the states of the converter operation and the time duration of each state. During the states, the components conditions change (the conditions consist of charging and discharging of inductors and capacitors or diodes on and off states [1–10]. Section 3 contains the conditions and the states with which analyses are done). Thus, the switch's duty cycle is the essential parameter in analysis of the converter equations such as voltage gain, voltage stress on the components and current of the components.

3 Operation principle of the proposed converter

The converter has one switch that means, its operation includes turn on and turn off stages due to the switching conditions. The components are assumed ideal and the operation stages for the switch are shown in Fig. 2.

To study the operation principle of the converter, it is assumed that the converter operates in continuous conduction mode (CCM) mode. When the PWM signal is equal to one, the switch turns on and current flows in different parts of the converter as shown in Fig. 2*a*. The diode D_1 blocks and prevents current flowing from source into the inductors. Furthermore, D_3 blocks the ways of short circuiting C_3 and C_4. According to the equivalent circuit in Fig. 2*a*, the state makes four possible loops during the operation. The first and the second loops consist of L_1–C_1 and L_2–C_2, respectively. The capacitors (C_1 and C_2) discharge and energise inductors (L_1 and L_2) in the loops. The third and fourth loops consist of C_1, D_2, C_4, R, C_2 and C_1, C_3, D_4, R, C_2. Using the loops in Fig. 2*a*, circuit equations can be written as below:

$$\begin{aligned} v_{L1} = v_{L2} = v_{C1} = v_{C2} \rightarrow v_C = v_L v_{C3} \\ = v_{C4} \;\&\; v_{C1} + v_{C2} = v_{C5} \rightarrow \quad v_{C5} = 2v_C \\ v_o = v_{C3} + v_{C5} = \; v_{C4} + v_{C5} \end{aligned} \tag{3}$$

where v_{L1}, v_{L2}, v_{C1}, v_{C2}, v_{C3}, v_{C4} and v_{C5} are voltage of the Z-source inductors (L_1 and L_2), voltage of the Z-source capacitors (C_1 and C_2) and voltage of the other capacitors (C_3, C_4 and C_5), respectively. When the switch turns off, the equivalent circuit changes as shown in Fig. 2*b*. In this state, D_2 and D_4 are blocking and the other diodes (D_1 and D_3) are conducting. During this state, current flows into the inductors and capacitors of the Z-source network (L_1, L_2, C_1 and C_2). Conduction of D_1 makes the loops between the components in which L_1 and L_2 discharge and energise C_1 and C_2, respectively. Furthermore, V_{in} takes part in the capacitors charge during the state. There are the other loops as L_1, C_2, C_5, D_3 and C_3. Based on the equivalent circuit, the following equations can be derived:

$$\begin{aligned} v_{C5} = v_{in} + v_{C3} \rightarrow v_{C3} = 2v_C - v_{in} \\ v_L = \; v_{in} - v_C \end{aligned} \tag{4}$$

Operation equations of the converter are obtainable by steady-state analysis. Voltage second balance equation of the inductors leads to finding the voltage gain of the converter. The balance equations consider that average voltage of the inductors during their charging and discharging are equal to zero. By assuming DC values of v_{in} and v_c as V_{in} and V_C, the average voltage equation for L_1 is

$$DV_C + (1-D)(V_{in} - V_C) = 0 \rightarrow V_C = \frac{1-D}{1-2D} V_{in} \quad (5)$$

Substituting (5) into (4), V_{C3} can be described by V_{in}

$$V_{C3} = V_{C4} = \frac{1}{1-2D} V_{in} \quad (6)$$

Substituting (6) into (3), voltage gain of the converter is as below:

$$M = \frac{V_o}{V_{in}} = \frac{3-2D}{(1-2D)} \quad (7)$$

where the range of the duty cycle is $0 < D < 0.5$. Equation (7) shows the converter voltage gain is higher or equal to 3 (in $D = 0$, M is 3). Boosting mode has the highest values per duty cycles close to 0.5. Considering the equivalent series resistance (ESR) effects, the converter can raise voltage gain until 11 per $D = 0.4$. Following parts describe the other quality factors of the converter.

3.1 Voltage stress on the components

Most of the components suffer from reverse voltage in power electronic converters. During design and implementation, voltage stress should be considered and reduced [1–4, 8]. Hence, it has been investigated in this part as one of the main factors. The capacitors have to withstand voltage stress values obtained by the following equations. Voltages of $C1$ and $C2$ are equal and by substituting (7) into (5), their voltage stress is

$$V_{C1} = V_{C2} = V_C = \frac{1-D}{(3-2D)} V_o \quad (8)$$

Substituting (7) into (6) gives C_3 and C_4 voltage stress as (9). Also, voltage of C_5 (the other parallel capacitor with the load) is equal to $2V_C$, thus, its voltage stress is twice the (8)

$$V_{C3} = V_{C4} = \frac{1}{(3-2D)} V_o \quad (9)$$

To choose appropriate components for the converter, inverse voltage of the switch and diodes have to be calculated. When the switch is turned off, its voltage is equal to $V_{C3} = 2V_C - V_{in}$ (Fig. 2*b*). Therefore, its voltage stress is

$$V_{Switch} = \frac{1}{(3-2D)} V_o \quad (10)$$

Similar methods are used for the diodes and their voltage stress is defined as below:

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = \frac{1}{(3-2D)} V_o \quad (11)$$

3.2 Inductor design

Using the current analysis makes calculation of inductors size possible. Design of the inductors can be done based on current ripple limitation or required minimum inductance for CCM [2, 3, 10]. Using the first stage equivalent circuit (Fig. 2*a*), the following equations can be written:

$$i_{C1} = i_{C2} = i_C \quad \& \quad i_{L1} = i_{L2} = i_L \quad (12)$$

$$i_{C5on} = i_o + i_L - i_{Con} \quad (13)$$

where i_{C5on} and i_{Con} are the capacitors current during the switch on state. Current of capacitor C_5 can be used to obtain inductors average current. Hence, the capacitor current during off state (Fig. 2*b*) is analysed

$$i_{C5off} = i_o - i_{inof} - i_{Coff} + i_L \quad (14)$$

where i_{C5off}, i_{inoff} and i_{Coff} are the components current during the switch off state. Current second balance equation of C_5 is

$$Di_{C5on} + (1-D) i_{C5off} = 0 \quad (15)$$

Substituting (13) and (14) into (15), inductors average current are obtained as below:

$$i_{L1} = i_{L2} = i_L = \frac{2V_o}{(1-2D)R_o} \quad (16)$$

To achieve inductance equations, voltage of L_1 is assumed in turn on interval

$$\begin{cases} L\dfrac{di_L}{dt} = V_L \\ dt = DT_S \quad \text{and} \quad di_L = \Delta I_L \end{cases} \quad (17)$$

Substituting (5) into (3), the inductors voltage are

$$V_L = \frac{1-D}{(1-2D)} V_{in} \quad (18)$$

Using (17) and (18), inductance and current ripple of L_1 are equal to

$$L_1 = L_2 = L = \frac{D(1-D)}{(1-2D)\Delta I_L f_s} V_{in} \quad (19)$$

$$\Delta I_L = \frac{D(1-D)}{(1-2D)L f_s} V_{in} \quad (20)$$

where f_s is switching frequency. Equation (19) determines the inductors size per a definite current ripple that can be chosen by the designer.

In DC–DC converters, inductor current has triangular waveform. Its average is equal to $\Delta I_L/2$ on the boundary of current continuous and discontinuous modes ($I_{Lmin} = 0 \rightarrow I_L = \Delta I_L/2$ and average current of the inductors are equal to (16)). So, by substituting (16) into (20), minimum required inductance can be calculated as below:

$$L_{1min} = L_{2min} = \frac{(2D^3 - 3D^2 + D)R_o}{4(3-2D)f_s} \quad (21)$$

Design of the inductors according to minimum inductance is a cost-effective method. To ensure current continuous mode of the inductors, the worst condition has to be noticed in calculation of L_{min}.

4 Comparison with other converters

To prove the proposed converter advantages, the analysed quality factors are compared with other converters. This section presents comparison between the proposed converter and the other converters including: conventional converters and the converter in [2], the number of components of which is equal to the proposed converter. The comparison is focused on boosting ability (voltage gain), voltage stress on the components and minimum inductance of the inductors.

4.1 Comparison of voltage gain

Fig. 3 depicts voltage gain curves of the converter and the compared ones. The curves are drawn based on the equations in Table 1. It can be seen (Fig. 3) that the proposed converter boosts input voltage with the highest voltage gain during the whole duty cycles. The excellence occurs from the beginning and duty cycle equal to zero. Furthermore, the proposed converter starts boosting voltage from $M = 3$ and the others start from $M \leq 2$. Quadratic boost converter and Z-source DC–DC converter have $M = 2$ in D

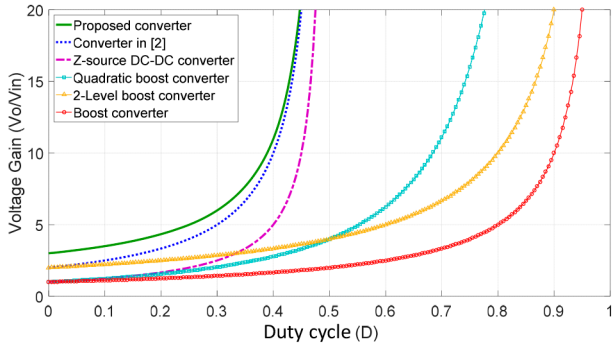

Fig. 3 *Voltage gain variations per different duty cycles for the compared converters*

Table 1 Comparisons among the proposed converter and the other converters

Converters	Voltage gain	Amount of inductors	Amount of capacitors	Amount of diodes	Amount of power switches	Maximum voltage stress across diodes	Maximum voltage stress across power switches	Common ground
boost converter	$1/(1-D)$	1	1	1	1	V_o	V_o	yes
quadratic boost converter	$1/(1-D)$^2	2	2	3	1	V_o & $(1-D)V_o$	V_o	yes
Z-source DC–DC converter	$1/(1-2D)$	2	3	2	1	V_o	V_o	no
converter in [2]	$2/(1-2D)$	2	5	4	1	$V_o/2$	$V_o/2$	yes
proposed converter	$(3-2D)/(1-2D)$	2	5	4	1	$V_o/(3-2D)$	$V_o/(3-2D)$	yes

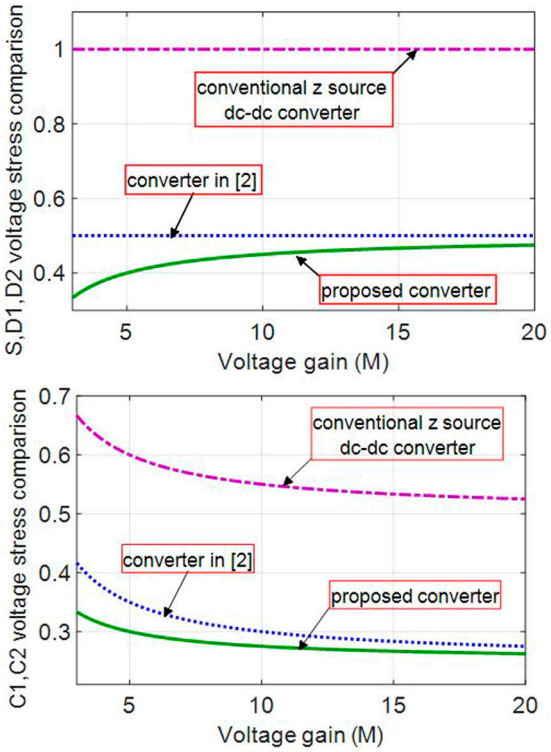

Fig. 4 *Voltage stress on the switch, D_1, D_2, C_1, C_2 for the proposed converter, the converter in [2] and conventional Z-source converter*

equal to 0.29 and 0.25, respectively. In addition, the proposed converter arises its voltage gain with the highest slope and it arrives to its maximum voltage gain in the lowest duty cycle in comparison to the others.

4.2 Voltage stress comparison

For the proposed converter, voltage stress on the switch and diodes depend on the duty cycle. Per duty cycles from $D=0$ to $D=0.5$, voltage stress of the proposed converter is lower or equal to the compared converters. According to the equations in Table 1, voltage stress for converter in [2] and the proposed converter have relation with duty cycles. As shown in Fig. 3, the mentioned converters operate in the range of $0<D<0.45$. The proposed converter imposes voltage stress in the range of $V_o/3$ (per $D=0$) to $V_o/2.1$ (per $D=0.45$).

The proposed converter has similarities in its operation with the converter in [2]. Hence, voltage stress on their similar semiconductors and capacitors are drawn in Fig. 4. Since the base of the proposed converter is Z-source network, Fig. 4 contains

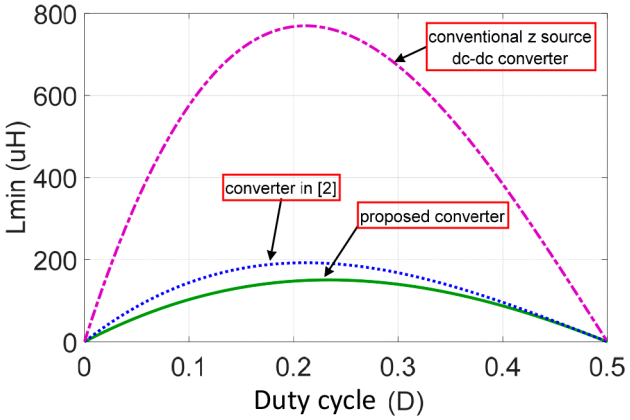

Fig. 5 *L_{min} of the proposed converter and the two compared converters – R_o = 400 Ω, f_s = 25 kHz*

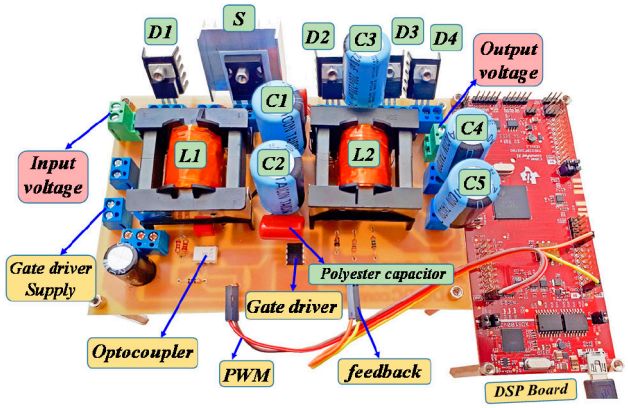

Fig. 6 *Prototype of the proposed converter and DSP board*

Table 2 Components and their parameters used for power loss calculation

	MOSFET	Diodes	Inductors
type	IRFP260N	MBR10200CT	Core: ETD39 N87 ferrite core
parameters	r_{DS} = 0.04 Ω	$r_D \simeq$ 0.04 Ω	r_L = 0.1 Ω
	$t_r + t_f$ = 108 nS	$t_{rr} \simeq$ 100 nS	
	V_{DS} = 200 V	V_F = 0.8 V	
	I_D = 50 A	V_{AK} = 200 V, I_D = 10 A	
other properties	R_o = 400 Ω, f_s = 25 kHz, V_{in} = 30 V, r_C = 0.01 Ω		

voltage stress of conventional Z-source converter. Voltage stress of the semiconductors in the conventional Z-source converter and the converter in [2] are higher than the proposed converter during the whole duty cycle range (Fig. 4). From Fig. 4, it can be seen that the proposed converter imposes lower voltage stress on the capacitors especially in $M < 10$. In practice, the proposed converter operates until $M = 10$ that shows the voltage stress reduction occurs in an effective range.

4.3 Choosing the inductor

Passive components determine the converter size and volume [9]. Inductors of DC–DC converters are bulky and designers try to reduce inductors size. Inductors can be designed for CCM or to limit the maximum current ripple [2, 3, 10]. Furthermore, inductors ESR impact the converters efficiency that should be controlled by proposing converters with smaller inductors [8]. Equation (21) defines L_{min} for the proposed converter. For the two other converters, L_{min} are calculated as below.

L_{min1} for conventional Z-source converter:

$$L_{min1} = \frac{(2D^3 - 3D^2 + D)R_o}{2f_s} \tag{22}$$

L_{min2} for the converter in [2]:

$$L_{min2} = \frac{(2D^3 - 3D^2 + D)R_o}{8f_s} \tag{23}$$

To compare the converters inductors, their L_{min} per different duty cycles are plotted in Fig. 5. From Fig. 5, it can be seen that the proposed converter needs lower minimum inductance per the whole duty cycles. For the worst case, L_{min} of the proposed converter, the converter in [2] and conventional Z-source converter are 180, 200 and 790 µH, respectively.

5 Experimental results

The experimental setup is presented in Fig. 6. Table 2 contains technical information about the used components. It has to be noticed to reduce skin effect and coil resistance, four strings wires are twisted (resistances of the coils are 0.1 Ω). The inductors are chosen 700 µH to limit the current ripple (based on (20)) in the worst case (this means L_{min} is not selection criteria here). In addition, C_1, C_2, C_3 and C_4 are all equal to 220 µF and their nominal voltage is 200 V.

Fig. 7 depicts the experimental results for the proposed Z-source converter. The results consist of quality factors of the converter operation as output voltage, voltage stress on the components and the inductors current ripples.

According to (7), output voltage has to be 180 V for $V_{in} = 30$ V and $D = 0.3$. The value in the experiment is 173.6 V (Fig. 7*a*) that has 3.5% difference with the theoretical value. The difference is because of parasitic components and voltage drop on the semiconductors. Using (10) and (11), voltage stress on the diodes and the switch are similar and equal to 72.3 V for $V_0 = 173.6$ and $D = 0.3$. Experimental results show that voltage stress on D_1, D_2, D_3, D_4 and the switch are in the range of 72.4–73.5 V (Figs. 7*b* and *c*). Voltage stress on capacitors C_1, C_2, C_3, C_4 and C_5 are 51.1, 50.9, 72.1, 72.4 and 102.9 V, respectively (Figs. 7*a* and *b*) which have to be 50.63 V for $C_1 = C_2$, 72.33 V for $C_3 = C_4$ and 101.26 V for C_5 ((8) and (9)).

According to (20), inductors current ripple has to be 0.9 A, that is 0.86 A approximately (Fig. 7*d*). The inductors continuous current mode proves that the used design method for the inductors is suitable (the converter operates near maximum duty cycles). It also operates with continues conduction mode in higher duty cycles. The converter voltage gain differs from 3 to 9 with high efficiency (Figs. 8*a* and *b*). Its efficiencies per $M = 3.3$ ($D = 0.1$) and $M = 7.5$ ($D = 0.365$) are 97.5 and 90%, respectively, that presents effective operation of the converter in boosting mode. Fig. 8*c* depicts efficiency as a function of output power.

The proposed converter is designed for renewable energy applications with low power. The converter operates with efficiency above 90% (Fig. 8*c*) for output power until 125 W.

In the next experiment, a proportional–integral controller is used to control and regulate output voltage on 220 V during load variation. The results in Figs. 9 and 10 demonstrate that the controller has been well designed. The controller has very fast response to load variation and input voltage variation in transient conditions. In Fig. 10, input voltage is varied during a short time from 12 to 32.5 V and controller tracks the changes fast with output voltage regulation. In the next step, input voltage is decreased from 32.5 to 14 V and the controller regulates output voltage similar to the previous step. Voltage regulation per changes illustrates the controller operation quality and the results demonstrate its well designing (Fig. 10).

The converter transfers power ≤ 125 W with efficiency more than 89% which proves its suitable operation for high voltage gains (during the experiments voltage gain is 7.33). From Fig. 9, it can be seen that output power per $D = 0.34$ and $D = 0.36$ are 50 and 187.5 W, respectively. The result shows that a small change in duty

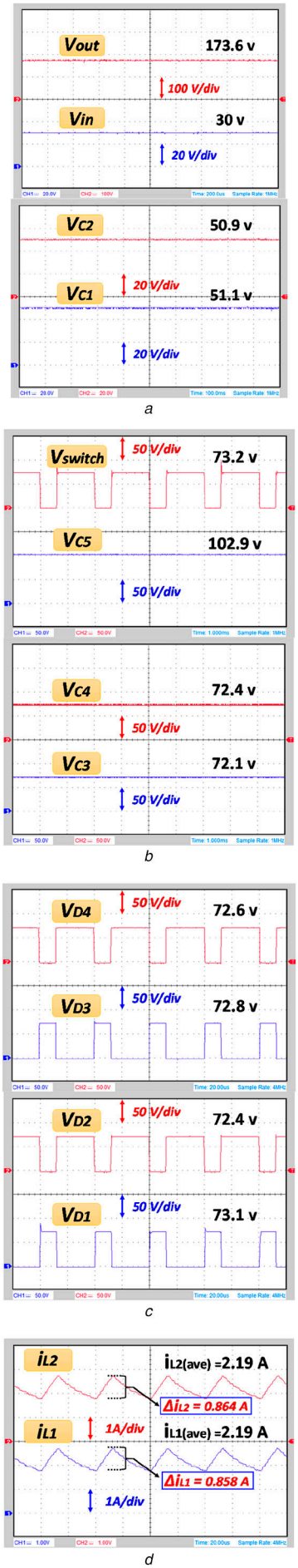

Fig. 7 *Experimental results of the proposed Z-source converter – per duty cycle equal to 0.3 and R_O = 400 Ω*

(a) Output voltage (V_{out}), input voltage (V_{in}), voltage of the capacitors C_1 and C_2 , ***(b)*** Voltage of the power switch (V_{switch}) and voltage of the capacitors C_3, C_4 and C_5, ***(c)*** Voltage of the diodes D_1, D_2, D_3 and D_4,***(d)*** Inductors current (i_{L1} and i_{L2})

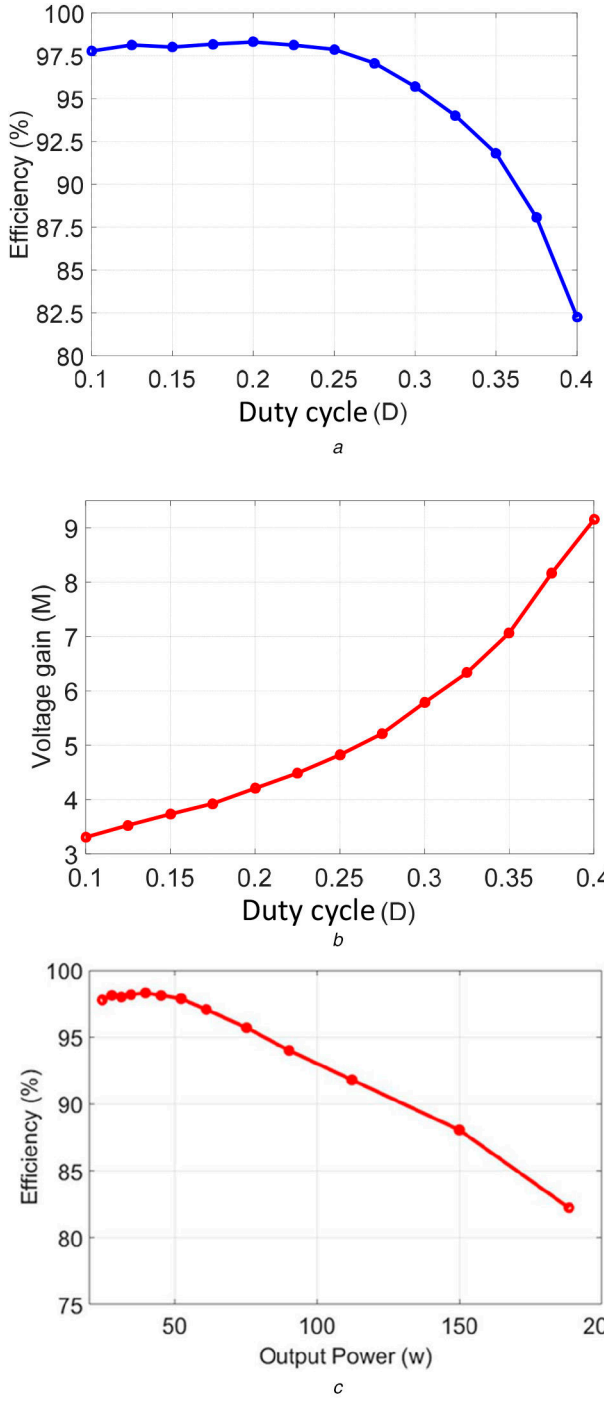

Fig. 8 *Quality factor curves of the proposed converter for various conditions*
(a) Efficiency per different duty cycles, ***(b)*** Voltage gain per different duty cycles, ***(c)*** Efficiency of the converter as a function of output power

cycle gets tripled output power. Thus, for a constant input and output voltages, the converter transfers power with high efficiency for a wide range of load variation. In addition, when input voltage increases, the controller regulates voltage per lower duty cycles with higher efficiencies (Fig. 8*a*).

6 Conclusion

The proposed DC–DC converter is a combination of reformed conventional Z-source and a switched capacitor. The converter is common grounded and it boosts input voltage until nine times. Furthermore, its voltage gain range for efficiencies more than 90% is 3–7.5. Its efficiencies per $M = 3.3$ ($D = 0.1$) and $M = 7.5$ ($D = 0.365$) are 97.5 and 90%, respectively, that presents effective operation of the converter in boosting mode. In comparison to

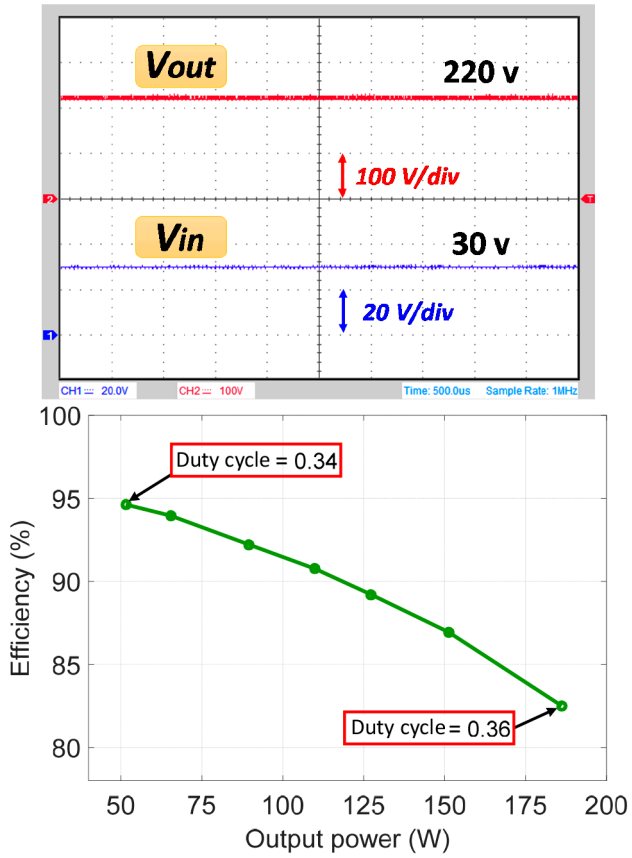

Fig. 9 *Efficiency of the converter during load variation and its regulated voltage on 220 V*

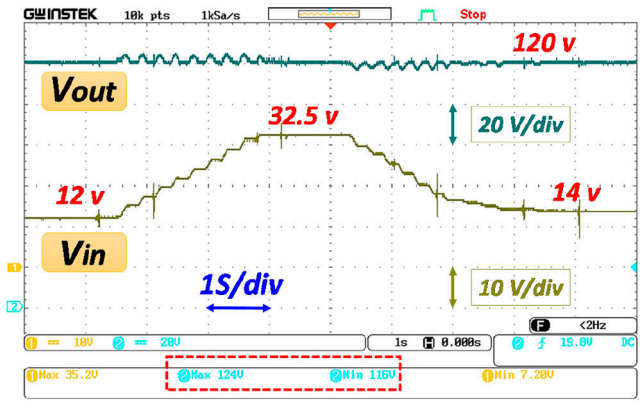

Fig. 10 *Controller operation during input voltage variations (to show its ability in transient conditions)*

similar converters, it has higher voltage gain per equal duty cycles. In addition, it operates in boosting mode with higher maximum voltage gain and it is appropriate for applications where low voltage sources are used.

According to the analysis, the proposed converter imposes lower voltage stress on its components in comparison to conventional Z-source converter and the converter in [2]. This advantage is valid during the whole duty cycle range. From the results, it can be seen that voltage stress on C_1 and C_2 are less than $0.32V_o$. In addition, voltage stress on the switch, D_1 and D_2 are less than $0.5V_o$. To validate the analysis, voltage stress on the semiconductors and the capacitors are investigated by experimental results that show the analysis and the experiments are in a good accordance with each other.

The converter needs smaller inductors that is concluded from the compared minimum inductances size. This means less parasitic effects leading to an improvement in the proposed structure.

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7 References

[1] Aquino, R.N.A.L.S., Tofoli, F.L., Praca, P.P., *et al.*: 'Soft switching high-voltage gain dc–dc interleaved boost converter', *IET Power Electron.*, 2015, **8**, (1), pp. 120–129

[2] Zhang, Y., Summer, C., Fu, M., *et al.*: 'A wide input-voltage range quasi-Z-source boost DC–DC converter with high-voltage gain for fuel cell vehicles', *IEEE Trans. Ind. Electron.*, 2018, **65**, (6), pp. 5201–5212

[3] H, Choi, , M, Jang, , M, Ciobotaru, , *et al.*: 'Performance evaluation of interleaved high- gain converter configurations', *IET Power Electron.*, 2016, **9**, (9), pp. 1852–1861

[4] Revathi, B.S., Mahalingam, P.: 'Non-isolated high gain DC–DC converter with low device stress and input current ripple', *IET Power Electron.*, 2018, **11**, (15), pp. 2553–2562

[5] Wu, T.F., Chang, Y.D., Chang, C.H., *et al.*: 'A 5 kW boost converter with various passive/active snubbers for reducing component stress and achieving high efficiency'. Proc. Int. Conf. Power Electronics Drives Systems, Taipei, Taiwan, November 2009, pp. 187–192

[6] Tofoli, F.L., de Castro Pereira, D., Josias de Paula, W., *et al.*: 'Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter', *IEEE Trans. Power Electron.*, 2015, **8**, (10), pp. 2044–2057

[7] Luo, F.L., Ye, H.: 'Positive output cascade boost converters', *Proc. Inst. Elect. Eng., (IEE) Electr. Power Appl.*, 2004, **151**, (5), pp. 590–606

[8] Mahmoudi, M., Ajami, A., Babaei, E.: 'A non-isolated high step-up DC-DC converter with integrated 3 winding coupled inductor and reduced switch voltage stress', *Int. J. Circ. Theor. Appl.*, 2018, **46**, (10), pp. 1879–1898

[9] Revathi, B.S., Mahalingam, P.: 'Transformerless high-gain DC–DC converter for microgrids', *IET Power Electron.*, 2016, **9**, (6), pp. 1170–1179

[10] Lee, S.W., Do, H.L.: 'Quadratic boost DC–DC converter with high voltage gain and reduced voltage stresses', *IEEE Trans. Power Electron.*, 2018, **34**, (3), pp. 2397–2404

[11] Zhang, N., Sutanto, D., Muttaqi, K.M., *et al.*: 'High-voltage-gain quadratic boost converter with voltage multiplier', *IET Power Electron.*, 2015, **8**, (12), pp. 2511–2519

[12] Rosas-Caro, J.C., Valdez-Resendiz, J.E., Mayo-Maldonado, J.C., *et al.*: 'Quadratic buck–boost converter with positive output voltage and minimum ripple point design', *IET Power Electron.*, 2018, **11**, (6), pp. 1306–1313

[13] Chang, Y.H., Chen, Y.J.: 'A switch-utilization-improved switched-inductor switched-capacitor converter with adapting stage number', *Int. J. Circ. Theor. Appl.*, 2016, **44**, (3), pp. 709–728

[14] Tang, Y., Fu, D., Wang, T., *et al.*: 'Hybrid switched-inductor converters for high step-up conversion', *IEEE Trans. Ind. Electron.*, 2015, **62**, (3), pp. 1480–1490

[15] Abutbul, O., Gherlitz, A., Berkovich, Y., *et al.*: 'Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit', *IEEE Trans. Circuits Syst. I, Fund. Theory Appl.*, 2003, **50**, (8), pp. 1098–1102

[16] Liang, T.J., Chen, S.M., Yang, L.S., *et al.*: 'Ultra-large gain step-up switched-capacitor dc–dc converter with coupled inductor for alternative sources of energy', *IEEE Trans. Circuits Syst. I, Regul. Pap.*, 2012, **59**, (4), pp. 864–874

[17] Maalandish, M., Hosseini, S.H., Ghasemzadeh, S., *et al.*: 'Six-phase interleaved boost dc/dc converter with high-voltage gain and reduced voltage stress', *IET Power Electron.*, 2017, **10**, (14), pp. 1904–1914

[18] Fekri, M., Molavi, N., Adib, E., *et al.*: 'High voltage gain interleaved DC–DC converter with minimum current ripple', *IET Power Electron.*, 2017, **10**, (14), pp. 1924–1931

[19] Peng, F.Z.: 'Z-source inverter', *IEEE Trans. Ind. Appl.*, 2003, **39**, pp. 504–510

[20] Zhang, J., Ge, J.: 'Analysis of Z-source dc–dc converter in discontinuous current mode'. Proc. Asia-Pacific Power and Energy Engineering Conf. (APPEEC), Chengdu, People's Republic of China, March 2010, pp. 1–4

[21] Zhu, M., Yu, K., Luo, F.L.: 'Switched inductor Z-source inverter', *IEEE Trans. Power Electron.*, 2010, **25**, (8), pp. 2150–2158

[22] Shindo, Y., Yamanaka, M., Koizumi, H.: 'Z-source DC-DC converter with cascade switched capacitor'. Proc. 37th Annual Conf. IEEE Industrial Electronics Society, Melbourne, VIC, Australia, November 2011, pp. 1665–1670

[23] Tang, Y., Xie, S., Zhang, C.: 'An improved Z-source inverter', *IEEE Trans. Power Electron.*, 2011, **26**, (12), pp. 3865–3868

[24] Tang, Y., Xie, S., Zhang, C., *et al.*: 'Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability', *IEEE Trans. Power Electron.*, 2009, **24**, (2), pp. 409–415

[25] Cao, D., Peng, F.Z.: 'A family of Z-source and quasi-Z-source dc–dc converters'. Proc. IEEE Applied Power Electronics Conf., Washington, DC, USA, February 2009, pp. 1093–1101